METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based on Japanese Patent Application No. 2006-219477 filed on Aug. 11, 2006, the disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a method for manufacturing a semiconductor device.

BACKGROUND OF THE INVENTION

[0003] Heretofore, there has been known a semiconductor device in which a super-junction structure is adopted for, for example, a power MOS transistor of vertical type. The "superjunction structure" is a configuration in which N type layers and P type layers to serve as a drift region are alternately arranged in the planar direction of a substrate. Owing to the adoption of such a structure, an electric field from a source toward a drain is also directed from the N type layers to the P type layers. Accordingly, the electric field can be prevented from concentrating in one place between the source and the drain, and in turn, the prevention of insulation breakdown can be attained.

[0004] Besides, as the width "dn" of each N type layer and the width "dp" of each P type layer are smaller, the concentrations of the respective layers can be made higher, and the ON-resistance of the semiconductor device can be made lower. Further, as the thicknesses of the respective layers are larger, a higher withstand voltage can be realized.

[0005] A method for forming the semiconductor device having the superjunction structure as stated above has been proposed in, for example, Patent Document 1 (JP-A-2005-317905 corresponding to USP Application Publication No. 2005/221547) and Patent Document 2 (JP-A-2005-294711 corresponding to EP 1734565-A1). Concretely, Patent Documents 1 and 2 have proposed the method wherein an N+ type substrate on which an epitaxial layer of N type is formed is prepared, and after trenches are formed in the substrate, epitaxial layers of P type are buried into the trenches, and the front surface of the substrate is flattened and polished, thereby to form the repeated structure of P type regions and N type regions.

[0006] When it is intended to lower the ON-resistance of the semiconductor device and to heighten the withstand voltage thereof, in the case of adopting the super-junction structure for the MOS transistor as stated above, it is considered to make smaller the width dn of each N type layer and the width dp of each P type layer and to make the respective layers thicker, as described above. However, when it is intended to realize the lower ON-resistance and the higher withstand voltage, it has been revealed by the inventors that problems to be stated below are posed.

[0007] As the first problem, for the purpose of manufacturing a device portion of high withstand voltage, the epitaxial layer of the N type on the N+ type substrate needs to be thickened. By way of example, the thickness of the N type epitaxial layer needs to be at least 30 μm for a withstand voltage of 600 V, and it needs to be at least 60 μm for a withstand voltage of 1200 V. In order to obtain such a large thickness, film formation for a long time is required, and a process cost becomes high.

[0008] Besides, as the second problem, when both the high withstand voltage and the low ON-resistance are to be attained, the widths dn and dp of the respective epitaxial layers of the N type and P type need to be made small so as to heighten the concentrations of the respective layers, and the respective layers need to be thickened. However, when the trench is narrowed in order to make small the width of, for example, the P type epitaxial layer, the P type epitaxial layer formed earlier at the opening part of the trench closes up this opening part of the trench, to incur the problem that the P type epitaxial layer is not formed at the bottom of the trench. Thus, a cavity appears within the trench, and the interior of the trench is not completely filled up with the P type epitaxial layer. In this case, in order to prevent the cavity from appearing, it is considered to bury the epitaxial layer from the bottom part of the trench. However, a long time is expended on film formation, and a process cost becomes high.

[0009] Further, as the third problem, for the purpose of realizing the high withstand voltage, the balance of (concentration×thickness), i.e., charge balance, needs to be adjusted in each of the layers. That is, the value of (concentration×dp) in the P type epitaxial layer and the value of (concentration×dn) in the N type epitaxial layer must be brought into coincidence. However, in forming the P type epitaxial layer within the trench, impurity ions migrate from the N+ type substrate into the P type epitaxial layer being formed, on account of an outward diffusion, and the concentration of the P type epitaxial layer deviates from a target value. It is accordingly difficult to adjust the concentrations and thicknesses of the respective layers so as to satisfy the charge balance.

[0010] Thus, it is required to form epitaxial layers constituting a super-junction structure, in a short time, thereby to curtail a manufacturing cost. Further, it is required to make smaller the widths of epitaxial layers constituting a super-junction structure, thereby to attain the higher withstand voltage and lower ON-resistance of a semiconductor device. Furthermore, it is required to attain a charge balance in respective layers constituting a super-junction structure, for the purpose of ensuring a high withstand voltage.

SUMMARY OF THE INVENTION

[0011] In view of the above-described problem, it is an object of the present disclosure to provide a method for manufacturing a semiconductor device.

[0012] According to a first aspect of the present disclosure, a method for manufacturing a semiconductor device includes: forming a plurality of trenches on a first side of a semiconductor substrate, wherein the substrate has a first conductive type; forming a second conductive type semiconductor film in each trench so that the substrate between two adjacent trenches provides a first column, and the second conductive type semiconductor film in each trench provides a second column, wherein the first and second columns are alternately repeated along with a predetermined direction in parallel to the first side of the substrate; thinning a second side of the substrate, the second side being opposite to the first side; and increasing an impurity concentration of the first conductive type in a thinned second side of the substrate so that a first conductive type layer is provided.